

A True 6F2 NOR Flash Memory Cell Technology - Impact of Floating Gate B4-Flash on NOR Scaling -

S. Shimizu, S. Shukuri, N. Ajika, T. Ogura, M. Mihara, Y. Kawajiri, K. Kobayashi and M. Nakashima
GENUSION, Inc., 7-1-3 Douicho, Amagasaki, Hyogo, Japan
Phone:+81-6-6416-6133, Fax:+81-6-6416-6134, e-mail:shukuri.shoji@genuision.co.jp

Abstract – This paper describes a true 6F2 B4-Flash (Back Bias assisted Band-to-Band tunneling induced Hot Electron injection Flash) memory cell, which is one half of conventional NOR cell, for the first time as a floating gate NOR cell. 6F2 B4-Flash cells featuring a self-aligned STI and self-aligned contact architectures have been fabricated by a 90nm process and was confirmed sufficient performance for NOR array operation. The cell size of 0.0486 μm^2 of 90nm 6F2 is the smallest NOR cell in the 90nm generation. B4-HE programming scheme, in which the voltage between drain and source sets to 1.8V, allows more aggressive gate length scaling than for conventional CHE programming cells, consequently gate length has been scaled down to 78nm.

Introduction

Increasing demand for high density low cost non-volatile memory applications requires continuous scaling for flash memories. The cell size of the conventional NOR flash memory utilizing channel hot-electron (CHE) programming has been scaled down maintaining cell size of 10F2[1][2](Fig.1) (F: minimum feature size). Although the self-aligned contact (SAC) technology has been applied in the 45nm generation[1], the cell size below 10F2 could not be realized. This is because the gate length still remains 110nm, because of the physical limitation of gate length scaling due to CHE programming. On the other hand, B4-HE programming allows aggressive gate length scaling down to below 90nm, thanks to the voltage between drain and source is only 1.8V[3]-[7].

In this work, a 90nm true 6F2 B4-Flash memory cells featuring a self-aligned STI and SAC technology are demonstrated. Obtained cell size of 0.0486 μm^2 is the smallest NOR cell in the 90nm generation, which is almost equivalent to that of a conventional 65nm NOR 10F2 cell. The 6F2 cell has been evaluated from the viewpoint of NOR array operation. Back bias dependencies of the cell performance and BTBT characteristics were also evaluated to confirm scalability of B4-Flash memory cell technology.

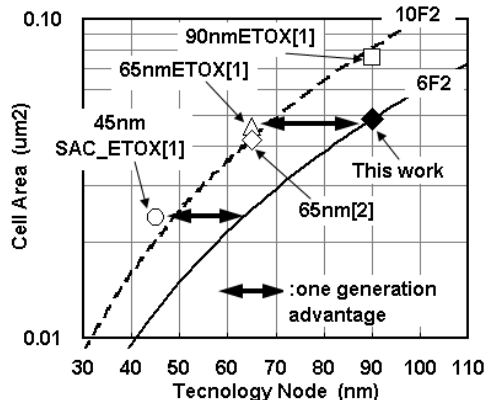


Fig.1 Trend of NOR cell size and impact of 6F2 cell.

B4 Programming Concept

Essential concept of B4 programming is that applying back bias leads the Y-circuit to operate within the power-supply voltage, consequently high speed reading and programming operation can be realized[3]-[5]. Cells are programmed by B4-HE injection and erased by uniform channel FN tunneling. Back bias required to generate B4-HEs has been scaled down to below 5V for 90nm cells from 8V for the 130nm cells[4]-[6].

6F2 Cell Structure

Layout of the 6F2 cell is simply characterized by a straight wordline of 3F pitch and bitline of 2F pitch(Fig.2). A floating gate self-aligned STI process and control gate self-aligned contact process have been employed in a 90nm process technology.

Thicknesses of the tunnel oxide and ONO dielectrics of the cells are 9nm and 13nm(oxide equivalent), respectively. Finished dimensions of gate and channel width are 90nm and 80nm, respectively(Fig.3). Asymmetrical BF2+ ion implantations for drain and source have been done to minimize BTBT hot-electron generation at the source junction.

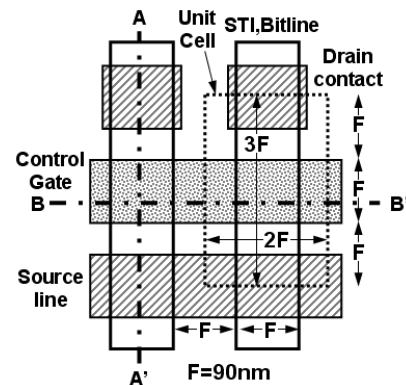


Fig.2 Schematic layout of 6F2 cell.

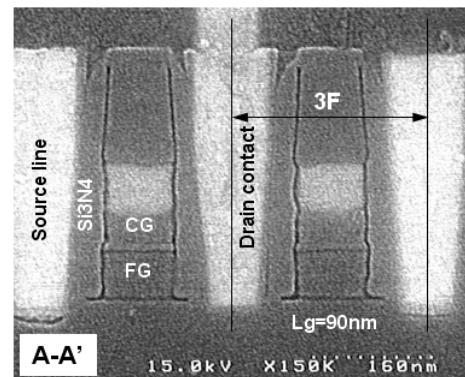


Fig.3(a) Cross sections of 90nm 6F2 cell in bitline direction.

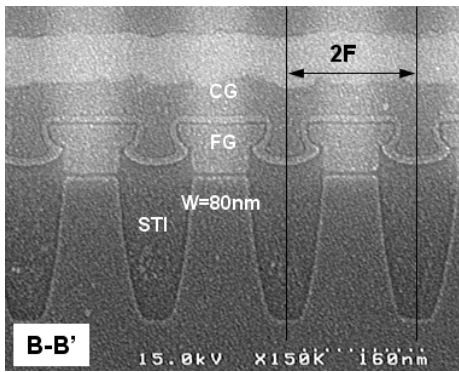


Fig.3(b) Cross sections of 90nm 6F2 cell in wordline direction.

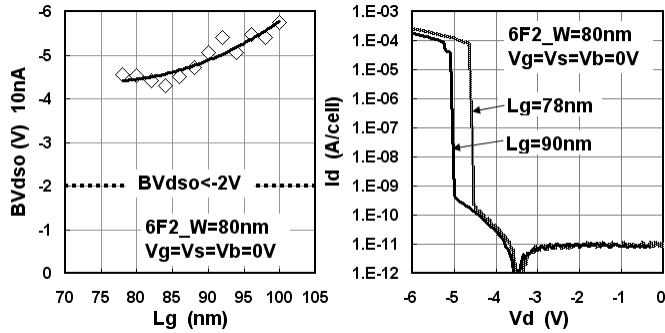


Fig.4 Gate length dependence of drain breakdown characteristics of the floating gate contacted device.

Scaling of the gate length down to 78nm has been performed by optimizing channel doping and drain junction profile. Even with 78nm gate length, breakdown voltage of the floating gate contacted devices is high enough ($< -4.5V$) for B4-HE programming(Fig.4).

6F2 Cell Characteristics

In NOR array architecture of 90nm B4-Flash memory, typical programming voltage condition is $V_{g_max}=12V$, $V_d=0V$, $V_s=1.8V$ and $V_b=4.4V$ (Fig.5). Un-selected cells in the selected bitline suffer with drain disturbance(DD), and un-selected cells in the selected wordline suffer with gate disturbance(GD). The inhibit-voltage has been carefully designed to maximize the disturbance immunity. The un-selected wordline voltage is 0V, and un-selected bitline is set to High-Z state[7]. The voltage of un-selected bitline goes up to around 3.6V by coupling to N-well, resulted in B4-HE generation at the drain junction is significantly suppressed.

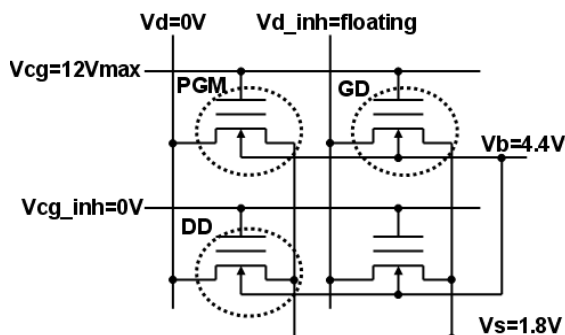


Fig.5 NOR array operation conditions for B4-Flash memory.

Programming time of the 6F2 cell with 90nm gate length is 10us, and drain and gate disturb lifetimes are around 10s(Fig.6). Therefore, the disturb margin (program time vs. disturb lifetime ratio) of the cell is $1E6$, which is sufficient for usual NOR array operation. It should be noted that two disturb lifetimes are well balanced.

Programming time of the 6F2 cell with 78nm gate length is 20us, and drain and gate disturb lifetimes are around 20s(Fig.7). The 6F2 cell of 78nm gate length also provides enough disturb margins as well as that of 90nm gate length cell.

Erase time in both 90nm cell and 78nm cell is around 2ms($V_{te}=-6V$) when $V_g=-19V$ (Figs.6,7).

Increasing of back bias achieves faster programming speed, however, the disturb lifetime becomes shorter more rapidly than programming time, consequently disturb margin degrades(Fig.8). Both cells with 90nm and 78nm gate length show almost the same back bias dependencies of programming time and drain disturb lifetime. It suggests that gate length dependency of B4-HE generation at the drain junction is quite small, which is attributed to the fact that B4-HE generation is well localized phenomena at the drain junction.

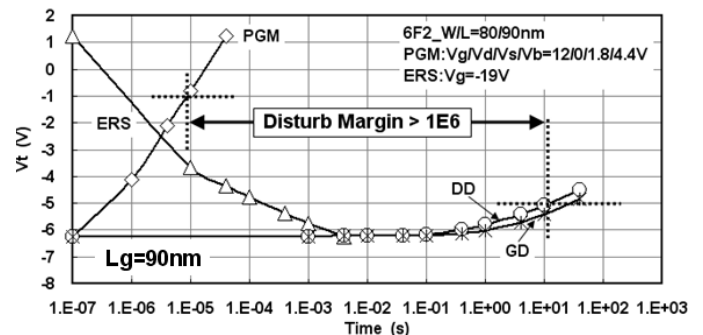


Fig.6 Cell characteristics of the 90nm gate length

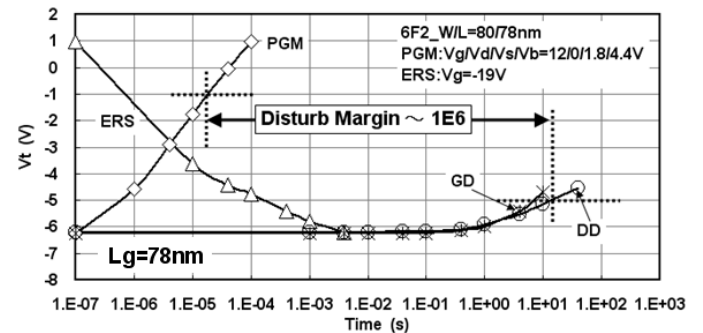


Fig.7 Cell characteristics of the 78nm gate length.

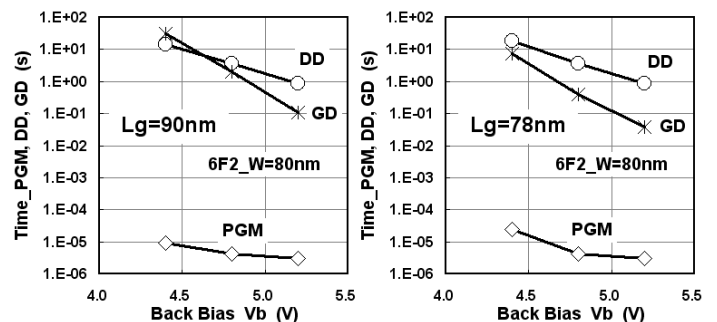


Fig.8 Back bias dependencies of programming time and disturb lifetime.

B4-HE programming current is estimated to be less than 10nA under the back bias between 4V and 6V, and is almost constant(Fig.9). Moreover, no increase in the programming current is seen even if the gate length is shortened from 90nm to 78nm. This result also suggests that the B4-HE generation is a localized phenomena near the drain junction and has enough margin for short channel effect.

The leakage current of the un-selected cell seems less than 1pA, which is below detectable limit. According to the programming current of 10nA/cell, the total current for 2k-byte simultaneous programming is expected to be smaller than 160uA, which means that the potential of extremely high speed programmability still maintains in the 78nm gate length cell.

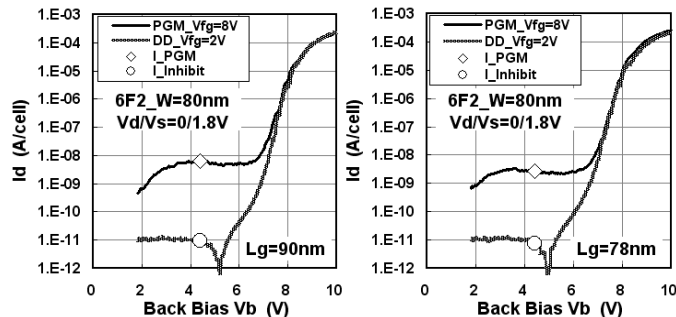


Fig.9 Programming BTBT drain leakage characteristics.

A very little degradation in the programming time by 10k-cycling is seen in the 78nm gate length cell(Fig.10). Vt change of the erased-state by 10k-cycling seems a little bit larger than that of a conventional N-channel NOR cell. However, the Vt window closure in the erased-state does not show the gate length dependency. These results imply that the gate length of B4-Flash memory cell is highly scalable from the viewpoint of cycling reliability.

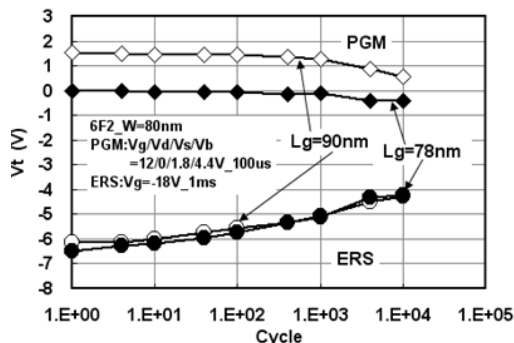


Fig.10 Program/erase cycling endurance.

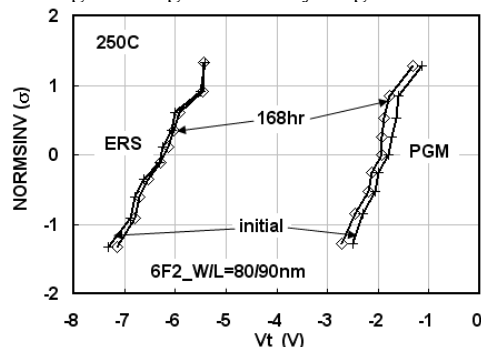


Fig.11 Intrinsic retention characteristics at 250C.

After 168hours storage at 250C, Vt shift is +70mV in the erased-state and -140mV in the programmed-state of the cells with P/E=2(Fig.11). This high-temperature intrinsic retention behavior of the initial cell is thought to be acceptable level for the practical use.

Conclusions

A 90nm true 6F2 B4-Flash memory cell as a floating gate NOR cell was successfully developed with cell size of 0.0486um², which is the smallest NOR cell in the 90nm generation, and is almost equivalent to that of a conventional 65nm 10F2 NOR cell. 6F2 B4-Flash cells featuring a self-aligned STI and self-aligned contact architectures have been fabricated by a 90nm process technology. Short channel margin of the gate length down to 78nm has been confirmed by optimizing channel doping and drain junction profile. Obtained cell shows excellent short channel margin and cycling endurance characteristics. 6F2 B4-Flash memory technology can greatly contribute to the progress of the high density low cost NOR type flash memory applications. Moreover, B4-HE programming scheme has a potential to achieve 5F2 cell by optimizing the gate slimming technique and an improved SAC process.

References

- [1] R. Fastow, R. Banerjee, P. Bjeletich, A Brand, H. Chao, J. Gorman, X. Guo, J.B. Heng, N. Koenigsfeld, S. Ma, A. Masad, S. Soss and B.J. Woo, "A 45nm NOR Flash Technology with Self-Aligned Contacts and 0.024um² Cell Size for Multi-level Applications", VLSI-TSA Technical Digest. pp.81-82, April 2008.
- [2] G. Sevali, D. Brazzelli, E. Camerlenghi, G. Capetti, S. Costantini, C. Cupeta, D. DeSimone, A. Ghetti, T. Ghilardi, P. Gulli, M. Mariani, A. Pavan and R. Somaschini, "A 65nm NOR Flash Technology with 0.042um² Cell Size for High Performance Multilevel Application", IEDM Technical Digest, pp.869-872, 2005.
- [3] S. Shukuri, N. Ajika, M. Mihara, K. Kobayashi, T. Endoh and M. Nakashima, "A 60 nm NOR Flash Memory Cell Technology Utilizing Back Bias Assisted Band-to-Band Tunneling Induced Hot-Electron Injection (B4-Flash)", Symposium on VLSI Tech., Technical Digest, pp.20-21, 2006.
- [4] S. Shukuri, N. Ajika, M. Mihara, Y. Kawajiri, T. Ogura, K. Kobayashi T. Endoh and M. Nakashima, "Floating Gate B4-Flash Memory Technology Utilizing Novel Programming Scheme -Highly Scalable, Efficient and Temperature Independent Programming-", Proceedings of NVSMW, pp.30-31, 2007.
- [5] M. Mihara, Y. Kawajiri, K. Kobayashi, T. Ogura, S. Shukuri, N. Ajika and M. Nakashima, "A 1.8V 4Mb Floating-Gate NOR Type B4-Flash Test Chip for 100MB/s Programming Speed", Proceedings of NVSMW, pp.23-24, 2007.
- [6] S. Shukuri, N. Ajika, S. Shimizu, M. Mihara, Y. Kawajiri, T. Ogura, K. Kobayashi and M. Nakashima, "Advantage of Floating Gate B4-Flash over Retention Reliability after Cycling -Characterization by Variation of Transconductance-", Proceedings of NVSMW, pp.16-19, 2008.
- [7] T. Ogura, M. Mihara, M. Kawajiri, Y. Kobayashi, S. Shimizu, S. Shukuri, N. Ajika and M. Nakashima, "A 90nm Floating Gate "B4-Flash" Memory Technology - Breakthrough of the Gate Length Limitation on NOR Flash Memory", Proceedings of NVSMW, pp.53-54, 2009.